What Is Claimed Is:

1. An array substrate device having a color filter-on-thin film transistor (COT) structure for a liquid crystal display device, comprising:

a gate line formed on a substrate along a transverse direction, the gate line including a gate pad at one end thereof;

a first insulating layer formed on the substrate to cover the gate line, the first insulating layer exposing a first portion of the gate pad;

a data line formed over the first insulating layer along a longitudinal direction on the substrate, the data line defining a pixel region with the gate line and including a data pad at one end thereof;

a thin film transistor formed at a crossing region of the gate and data lines, the thin film transistor including a gate electrode, a semiconductor layer, a source electrode, and a drain electrode;

a black matrix overlapping the thin film transistor, the gate line, and the data line except a second portion of the drain electrode;

a second insulating layer formed over an entire surface of the substrate to cover the black matrix, the second insulating layer exposing the first portion of the gate pad, a third portion of the data pad, and the pixel region;

a first pixel electrode within the pixel region and contacting the second exposed portion of the drain electrode;

a color filter on the first pixel electrode within the pixel region; and

a second pixel electrode on the color filter and contacting the first pixel electrode.

2. The device according to claim 1, further comprising an inorganic insulating layer between the thin film transistor and the black matrix.

3. The device according to claim 2, wherein the inorganic insulating layer includes one of silicon nitride and silicon oxide.

4. The device according to claim 3, wherein the inorganic insulating layer exposes the first portion of the gate pad and the third portion of the data pad.

5. The device according to claim 1, wherein the semiconductor layer includes an active layer of intrinsic amorphous silicon over the gate electrode and an ohmic contact layer of extrinsic amorphous silicon on the active layer.

6. The device according to claim 1, wherein the first and second pixel electrodes includes one of indium tin oxide and indium zinc oxide.

7. The device according to claim 1, wherein the color filter includes at least one of red, green, and blue colors.

8. The device according to claim 1, further comprising a storage metal layer on the first insulating layer over the gate line.

9. The device according to claim 8, wherein the second insulating layer exposes a fourth portion of the storage metal layer.

10. The device according to claim 9, wherein the first pixel electrode contacts the fourth portion of the storage metal layer exposed by the second insulating layer.

11. The device according to claim 8, wherein the storage metal layer and a portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

12. The device according to claim 1, wherein the first pixel electrode directly contacts the substrate.

13. A method of forming an array substrate having a color filter-on-thin film transistor (COT) structure for a liquid crystal display device, comprising:

forming a gate line on a substrate along a transverse direction, a gate pad at one end of the gate line, and a gate electrode extending from the gate line;

forming a first gate insulating layer on the substrate to cover the gate line, the gate pad, and the gate electrode;

forming an active layer of intrinsic amorphous silicon and an ohmic contact layer of extrinsic amorphous silicon layer in series on the first gate insulating layer over the gate electrode;

forming a data line, a data pad, a source electrode, and a drain electrode, the data line disposed perpendicularly crossing the gate line and defining a pixel region, the data pad disposed at one end of the data line, the source electrode extending from the data line on a first portion of the ohmic contact layer, and the drain electrode spaced apart from the source electrode on a second portion of the ohmic contact layer to form the thin film transistor;

forming a second insulating layer over an entire surface of the substrate to cover the thin film transistor;

forming a black matrix on the second insulating layers to cover the thin film transistor, the gate line, and the data line except a first portion of the drain electrode;

forming a third insulating layer over an entire surface of the substrate to cover the black matrix;

patterning the first, second, and third insulating layers to expose the first portion of drain electrode;

forming a first transparent electrode layer over an entire surface of the substrate to cover the patterned third insulating layer and contacting the exposed portion of the drain electrode;

forming a color filter on the first transparent electrode layer within the pixel region;

forming a second transparent electrode layer over an entire surface of the substrate to cover the color filter and the first transparent electrode layer;

patterning the first and second transparent electrode layers to form first and second pixel electrodes; and

patterning portions of the first, second, and third insulating layer over the gate and data pads to form gate and data pad contact holes, respectively, after forming the first and second pixel electrodes.

14. The method according to claim 13, wherein the thin film transistor includes the gate electrode, the active layer, the ohmic contact layer, the source electrode, and the drain electrode.

15. The method according to claim 13, wherein the first and second pixel electrodes form a sandwich pixel electrode.

16. The method according to claim 13, wherein the color filter is interposed between the first and second pixel electrodes.

17. The method according to claim 13, wherein the gate pad contact hole exposes a second portion of the gate pad, and the data pad contact hole exposes a third portion of the data pad.

18. The method according to claim 13, wherein the second insulating layer is interposed between the thin film transistor and the black matrix.

19. The method according to claim 13, wherein the first to third insulating layers include one of silicon nitride and silicon oxide.

20. The method according to claim 13, wherein the first and second transparent electrode layers includes at least one of indium tin oxide and indium zinc oxide.

21. The method according to claim 13, wherein the color filter includes at least one of red, green, and blue colors.

22. The method according to claim 13, wherein forming the data line includes forming a storage metal layer on the first insulating layer over the gate line.

23. The method according to claim 22, wherein the second and third insulating layers expose a fifth portion of the storage metal layer.

24. The method according to claim 23, wherein the first pixel electrode contacts the exposed fifth portion of the storage metal layer.

25. The method according to claim 22, wherein the storage metal layer and a portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

26. The method according to claim 13, wherein the first pixel electrode directly contacts the substrate.

27. An array substrate device having a color filter-on-thin film transistor (COT) structure for a liquid crystal display device, comprising:

a gate line formed on a substrate along a transverse direction, the gate line including a gate pad at one end thereof;

a first insulating layer formed on the substrate to cover the gate line, the first insulating layer exposing a first portion of the gate pad;

a data line formed over the first insulating layer along a longitudinal direction on the substrate, the data line defining a pixel region with the gate line and including a data pad at one end thereof;

a thin film transistor formed at a crossing region of the gate and data lines, the thin film transistor including a gate electrode, a semiconductor layer, a source electrode, and a drain electrode;

a black matrix overlapping the thin film transistor, the gate line, and the data line except a second portion of the drain electrode;

a second insulating layer formed over an entire surface of the substrate to cover the black matrix, the second insulating layer exposing the first portion of the gate pad, a third portion of the data pad, and the pixel region;

a first pixel electrode at the pixel region and contacting the exposed second portion of the drain electrode;

a color filter on the first pixel electrode at the pixel region;

a second pixel electrode on the color filter, contacting the first pixel electrode;

first and second gate pad terminals contacting the gate pad;

first and second data pad terminals contacting the data pad;

a first color filter pattern disposed between the first and second gate pad terminals; and

a second color filter pattern disposed between the first and second data pad terminals.

28. The device according to claim 27, further comprising an inorganic insulating layer between the thin film transistor and the black matrix.

29. The device according to claim 28, wherein the inorganic insulating layer includes one of silicon nitride and silicon oxide.

30. The device according to claim 29, wherein the inorganic insulating layer exposes the first portion of the gate pad and the third portion of the data pad.

31. The device according to claim 27, wherein the semiconductor layer includes an active layer of intrinsic amorphous silicon over the gate electrode and an ohmic contact layer of extrinsic amorphous silicon on the active layer.

32. The device according to claim 27, wherein the first and second pixel electrodes, the first and second gate pad terminals, and the first and second data pad terminals include at least one of indium tin oxide and indium zinc oxide.

33. The device according to claim 27, wherein the color filter and the first and second color filter patterns include at least one of red, green, and blue colors.

34. The device according to claim 27, further comprising a storage metal layer on the first insulating layer over the gate line.

35. The device according to claim 34, wherein the second insulating layer exposes a fourth portion of the storage metal layer.

36. The device according to claim 35, wherein the first pixel electrode contacts the fourth portion of the storage metal layer.

37. The device according to claim 34, wherein the storage metal layer and a fifth portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

38. The device according to claim 27, wherein the first pixel electrode directly contacts the substrate.

39. A method of forming an array substrate having a color filter-on-thin film transistor (COT) structure for a liquid crystal display device, comprising:

forming a gate line on a substrate along a transverse direction, a gate pad at one end of the gate line, and a gate electrode extending from the gate line;

forming a first gate insulating layer on the substrate to cover the gate line, the gate pad, and the gate electrode;

forming an active layer of intrinsic amorphous silicon and an ohmic contact layer of extrinsic amorphous silicon layer in series on the first gate insulating layer over the gate electrode;

forming a data line, a data pad, a source electrode, and a drain electrode, the data line disposed perpendicularly crossing the gate line and defining a pixel region, the data pad disposed at one end of the data line, the source electrode extending from the data line on a first portion of the ohmic contact layer, and the

drain electrode spaced apart from the source electrode on a second portion of the ohmic contact layer to form a thin film transistor at a crossing of the gate and data lines;

forming a second insulating layer over an entire surface of the substrate to cover the thin film transistor;

forming a black matrix on the second insulating layer and over the thin film transistor, the gate line, and the data line except a first portion of the drain electrode;

forming a third insulating layer over an entire surface of the substrate to cover the black matrix;

patterning the first, second, and third insulating layers to expose the first portion of drain electrode and to form a gate pad contact hole to the gate pad and a data pad contact hole to the data pad;

forming a first transparent electrode layer over an entire surface of the substrate to cover the patterned third insulating layer, the first transparent electrode layer contacting the exposed first portion of the drain electrode, the gate pad through the gate pad contact hole, and the data pad through the data pad contact hole;

forming a color filter and first and second color filter patterns on the first transparent electrode layer, the color filter disposed within the pixel region, and the

first and second color filter patterns disposed over the gate and data pads, respectively;

forming a second transparent electrode layer over an entire surface of the substrate to cover the color filter, the first and second color filter patterns, and the first transparent electrode layer; and

patterning the first and second transparent electrode layers to form first and second pixel electrodes, first and second gate pad terminals, and first and second data pad terminals.

40. The method according to claim 39, wherein the thin film transistor includes the gate electrode, the active layer, the ohmic contact layer, the source electrode, and the drain electrode.

41. The method according to claim 39, wherein the first and second pixel electrodes form a sandwich pixel electrode.

42. The method according to claim 39, wherein the color filter is interposed between the first and second pixel electrodes.

43. The method according to claim 39, wherein the first color filter pattern is interposed between the first and second gate pad terminals, and the second color filter pattern is interposed between the first and second data pad terminals.

44. The method according to claim 39, wherein patterning the first, second, and third insulating layers forms a plurality of gate pad contact holes exposing the gate pad and a plurality of data pad contact holes exposing the data pad.

45. The method according to claim 44, wherein the first color filter pattern is disposed within each gate pad contact hole.

46. The method according to claim 39, wherein forming the first and second color filter patterns includes a mask having a plurality of slits.

47. The method according to claim 46, wherein light passing through the plurality of slits is diffracted to form the first and second color filter patterns having a short height.

48. The method according to claim 39, wherein the second insulating layer is interposed between the thin film transistor and the black matrix.

49. The method according to claim 39, wherein the first, second, and third insulating layers include at least one of silicon nitride and silicon oxide.

50. The method according to claim 39, wherein the first and second transparent electrode layers include at least one of indium tin oxide and indium zinc oxide.

51. The method according to claim 39, wherein the color filter and the first and second color filter patterns include at least one of red, green, and blue colors.

52. The method according to claim 39, wherein forming the data line includes forming a storage metal layer on the first insulating layer over the gate line.

53. The method according to claim 52, wherein the second and third insulating layers expose a second portion of the storage metal layer.

54. The device according to claim 53, wherein the first pixel electrode contacts the exposed second portion of the storage metal layer.

55. The device according to claim 52, wherein the storage metal layer and a third portion of the gate line form a storage capacitor with the first insulating layer interposed between the storage metal layer and the gate line.

56. The device according to claim 39, wherein the first pixel electrode directly contacts the substrate.